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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,477	FURUHATA, TOMOYUKI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 24* is/are allowed.

6)☒ Claim(s) *1-5,7-14,16-21,23,25 and 28-32* is/are rejected.

7)☒ Claim(s) *15,22,26,27 and 33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 08 July 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-5,7,9,23, and 32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156).

Hirano discloses a semiconductor device comprising a semiconductor substrate 11 of a first conductivity (p) type having a memory region; a first well 12 of a second conductivity (n) type located in the memory region; and a second well 14 of a first conductivity (p) type located in the first well 12, the nonvolatile memory transistor including an n-type source and drain that are located in the second well 14, the non-volatile memory transistor is operated using voltages selected from the group consisting of positive and negative voltages, the operation includes writing and/or erasing data, writing data in the non-volatile memory transistor uses a voltage in an opposite polarity applied to the control gate, a voltage in one polarity applied to one of

the source and the drain, a voltage in the opposite polarity applied to the other of the source and the drain, a voltage in the opposite polarity applied to the second well 14, and a voltage in the one polarity applied to the first well 12, and for erasing data in the non-volatile memory transistor, a voltage in the one polarity applied to the control gate, a voltage in the opposite polarity applied to one of the source and the drain, a voltage in the opposite polarity applied to the other of the source and the drain, a voltage in the opposite polarity applied to the second well 14, and a voltage in the one polarity applied to the first well 12, data is written in the non-volatile memory transistor by channel hot electrons, data is erased by Fowler Nordheim Tunneling, the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the first gate insulation layer and the second gate insulation layer are located above the second well 14 and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer, alternatively, having a non-volatile memory transistor with a semiconductor substrate 11 of a first conductivity (p) type having a memory region; a first well 12 of a second conductivity (n) type located in the memory region; and a second well 14 of a first conductivity (p) type located in the first well 12 wherein the non-volatile memory transistor comprises a source, a drain, and

means for performing an data writing operation using a first voltage of a first polarity and a data erasing operation using a second voltage of a second polarity opposite from that of the first polarity. Note figure 3, tables 1 and 2, col. 2 ll. 9,22, col. 1 ll. 33,56,60, and col. 16 l. 34 of Hirano. Hirano discloses that the non-volatile memory transistor has a stacked gate structure but Hirano does not disclose that the non-volatile memory transistor has a split-gate structure. However, Takeda et al. discloses that a split gate may be directly substituted for a stacked gate in a memory transistor, and the advantages thereof. Note paragraphs 3 and 4 of Takeda et al. Therefore, it would have been obvious to one of ordinary skill in the art to replace the stacked gate structure of Hirano's memory cell with the split gate such as taught by Takeda et al. in order to prevent excess charge extraction from the floating gates during erase mode to thus prevent "constant on" channels and false data reads.

B. Claim 31 stands rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156) and THOMAS (6,242,773).

Hirano and Takeda et al. disclose a semiconductor memory device comprising a semiconductor substrate 11 of a first conductivity (p) type having a memory region; a first well 12 of a second conductivity (n) type located in the memory region; and a second well 14 of a first conductivity (p) type located in the first well 12, the nonvolatile memory transistor including an n-type source and drain that are located in the second well 14, a first gate insulation layer, a second gate insulation layer, a floating gate, a

control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the first gate insulation layer and the second gate insulation layer are located above the second well 14 and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer. Note figure 3, tables 1 and 2, col. 2 ll. 9,22, col. 1 ll. 33,56,60, and col. 16 l. 34 of Hirano. Note that, as explained above, it would have been obvious to one of ordinary skill in the art to replace the stacked gate structure of Hirano's memory cell with the split gate such as taught by Takeda et al. in order to excess charge extraction from the floating gates during erase mode to thus prevent "constant on" channels and false data reads. Hirano does not disclose that the intermediate insulation layer is composed of at least three insulation layers, wherein a first layer of the three insulation layers contacts the floating gate, a third layer contacts the control gate, and a second layer is located between the first and third layers.

However, Thomas discloses a non-volatile memory cell with an ONO intermediate insulation layer composed of at least three insulation layers 118 120 124, wherein a first layer 118 of the three insulation layers contacts the floating gate 116, a third layer 124 contacts the control gate 128, and a second layer 120 is located between the first and third layers 118 124. Note figure 1E of Thomas. Therefore, it would have been obvious to a person having skill in the art to replace the single layer of Hirano's memory cell with

the ONO layer such as taught by Thomas in order to allow the intermediate insulation layer and the floating gate to be simultaneously patterned and self-aligned on the control gate to thus provide better more efficient manufacture.

C. Claims 10,11,16-20,25, and 28-30 stand rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156), as applied to claim 9 above, and further in view of NAKAMURA et al. (5,654,577) and Ito et al. (5,650,344).

Hirano and Takeda et al. disclose a semiconductor memory device comprising a semiconductor substrate 11 of a first conductivity (p) type having a memory region; a first well 12 of a second conductivity (n) type located in the memory region; and a second well 14 of a first conductivity (p) type located in the first well 12, the nonvolatile memory transistor including an n-type source and drain that are located in the second well 14, a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein the first gate insulation layer and the second gate insulation layer are located above the second well 14 and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer. Note figure 3, tables 1 and 2, col. 2 ll. 9,22, col. 1 ll. 33,56,60, and col. 16 l. 34 of Hirano.

Hirano does not disclose that the semiconductor substrate include first, second and third transistor regions, the first transistor region including a first voltage-type transistor that operates at a first voltage level, the second transistor region including a second voltage-type transistor that operates at a second voltage level, and the third transistor region including a third voltage-type transistor that operates at a third voltage level, forming at least a flash-memory (flash EEPROM), wherein the flash memory includes a memory cell array composed of non-volatile memory transistors and peripheral circuits formed therein, and wherein the first voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit, the second voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit, and the third voltage-type transistor is included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

Further, Hirano does not disclose that the gate insulation layer of the second voltage-type transistor has at least two insulation layers and the gate insulation layer of the third voltage-type transistor has at least three insulation layers.

However, Nakamura et al. discloses a semiconductor integrated circuit device with a semiconductor substrate that includes first (input output), second (NMOS) and third (PMOS) transistor regions, the first transistor region includes a first voltage-type

transistor that operates at a first voltage level, the second transistor region includes a second voltage-type transistor that operates at a second voltage level, and the third transistor region includes a third voltage-type transistor that operates at a third voltage level, forming at least a flash-memory (flash EEPROM), the flash memory including a memory cell array composed of non-volatile memory transistors and peripheral circuits formed therein, and wherein the first and second voltage-type transistor are both included in circuits forming a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer, and a control circuit, and the third voltage-type transistor is included in a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit. Note figs. 1-4, col. 8 ll. 10-64, and col. 3 ll. 1-16 of Nakamura et al.

Further, Ito et al. discloses a method of making a MOSFET with a re-oxidized, nitrided gate insulation layer 21 having at least two insulation layers and in fact having three insulation layers. Note col. 1 ll. 19-20 of Ito et al.

Therefore, it would have been obvious to a person having skill in the art to augment Hirano's semiconductor memory device with the three region, three voltage peripherals such as taught by Nakamura et al., and the two and three layer onynitride and ONO gate insulators such as taught by Ito et al., in order to bias the PMOS circuitry separately from the I/O and NMOS circuitry, improving refresh rates, reducing leakage currents, protecting against undershoot, and ultimately raising peripheral circuit operation speed, and to provide better improve gate oxide quality with respect to charge

generation due to high field and radiation, retard boron diffusion from boron doped polysilicon gates, increase hot electron resistance, and increase the punch through voltage.

The applicant's claims 10, 11 and 16 do not distinguish over the Ito et al. reference regardless of the process used to form the various gate insulation layers, because only the final product is relevant, not the recited processes of a single step forming the gate insulation layer of the first voltage-type transistor, one of the second voltage-type transistor gate insulation layers, and one of the third voltage-type transistor gate insulation layers and a single step forming a layer of the third voltage-type transistor gate insulation layer and a layer of the intermediate insulation layer of the non-volatile memory transistor.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claim 18, although Ito et al.'s device does not teach the exact thick nesses of the second voltage-type transistor gate insulation layer as that claimed by Applicant, the thickness differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

With regard to claims 17,19, and 20, although Hirano's device does not teach the exact thicknesses of the first voltage-type transistor gate insulation layer, third voltage-type transistor gate insulation layer, and non-volatile memory transistor intermediate insulation layer as that claimed by Applicant, the thickness differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

D. Claims 12-14 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156), Ito et al. (5,650,344), and NAKAMURA et al. (5,654,577), as applied to claim 11 above, and further in view of THOMAS (6,242,773).

Hirano, Ito et al., and Nakamura et al. disclose all the limitations of claims 12-14 and 21 except that that the intermediate insulation layer is composed of at least three insulation layers, wherein a first layer of the three insulation layers contacts the floating

gate, a third layer contacts the control gate, and a second layer is located between the first and third layers. Note figure 3, tables 1 and 2, col. 2 ll. 9,22, col. 1 ll. 33,56,60, and col. 16 l. 34 of Hirano, col. 1 ll. 19-20 of Ito et al., and figs. 1-3, col. 8 ll. 10-64, and col. 3 ll. 1-16 of Nakamura et al.

However, Thomas discloses a non-volatile memory cell with an ONO intermediate insulation layer composed of at least three insulation layers 118 120 124, wherein a first layer 118 of the three insulation layers contacts the floating gate 116, a third layer 124 contacts the control gate 128, and a second layer 120 is located between the first and third layers 118 124. Note figure 1E of Thomas. Therefore, it would have been obvious to a person having skill in the art to replace the single layer of Hirano's memory cell with the ONO layer such as taught by Thomas in order to allow the intermediate insulation layer and the floating gate to be simultaneously patterned and self-aligned on the control gate to thus provide better more efficient manufacture.

The applicant's claims 12-15 do not distinguish over the Thomas reference regardless of the process used to form the intermediate insulation layers, the second outermost layer that contacts the control gate of the intermediate insulation layer and the gate insulation layer of the first voltage-type transistor, an insulation layer of the intermediate insulation layer, and the "silicon oxide layer" (presumed to refer to the insulation layer between first and second outer layers), because only the final product is relevant, not the recited processes of thermal oxidation method, single step, CM method, or CMP method (HTO or TEOS).

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claim 21, although Thomas's device does not teach the exact thicknesses of the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor, the second outermost layer, and the second layer formed between the first and the second outermost layers as that claimed by Applicant, the thickness differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

E. Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156), as applied to claim 1 above, and further in view of Lu et al. (4,688,063).

As discussed above with reference to claim 1, Hirano and Nakamura et al. disclose all the limitations of claim 8 except that that the source and drain have an impurity concentration of 1 - 8 x 10^{20} CM^{-3}, the second well has a surface impurity concentration of 0.5 - 5 x 10^{16} CM^{-3}, and the second well has a peak impurity concentration of 1 - 4 x 10^{17} CM^{-3}. Note figure 3, tables 1 and 2, col. 2 lines 9,22, col. 1 lines 33,56,60, and col. 16 line 34 of Hirano, and paragraphs 3 and 4 of Takeda et al.

However, Lu et al. discloses a memory cell with a source and drain that have impurity concentrations of 5 x 10^{19} CM^{-3} and 1 x 10^{20} CM^{-3}, and a well that has a surface impurity concentration of 2 x 10^{16} CM^{-3} and a peak impurity concentration of 1 x 10^{17} CM^{-3}. Note figure 1 and column 7 lines 5-18 and column 8 lines 56-59 of Lu et al.

Hirano and Takeda et al. disclose the claimed invention except for the precise doping of the source drain and second well. Hirano and Takeda et al. do not discuss doping ranges at all, leaving it to one having skill in the art to find optimum doping ranges using long established standards such as the ones disclosed by Lu et al. (note that Lu et al. was published more than ten years before Hirano and Takeda et al.) as starting points. It would have been obvious to one of ordinary skill in the art at the time the invention was made to reach the claimed impurity ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Allowable Subject Matter

3. Claims 15,22,26,27 and 33-35 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

A. Claim 6 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising a semiconductor substrate of a first conductivity type having a memory region, a first well of a second conductivity type located in the memory region, and a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well, wherein the non-volatile memory transistor is operated using voltages including positive and negative voltages, wherein, for writing data in the non-volatile memory transistor, a voltage in an opposite polarity is applied to the control gate, a voltage in one polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well, wherein, for erasing data in the non-volatile memory transistor, a voltage in the one polarity is applied to the control gate, a voltage in the opposite polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the

first well, wherein, for writing data in the non-volatile memory transistor, a voltage of -3 V through -4 V is applied to the control gate, a voltage of +3 V through +4 V is applied to one of the source and the drain, a voltage of -5 V through -6 V is applied to the other of the source and the drain, a voltage of -5 V through -6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well, and wherein, for erasing data in the non-volatile memory transistor, a voltage of +(V through +'7 V is applied to the control gate, a voltage of -5 V through -6 V is applied to one of the source and the drain, a voltage of -5 V through -6 V is applied to the other of the source and the drain, a voltage of -5 V through -6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well.

B. Claim 24 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a combination that includes at least non-volatile memory transistor having a split-gate structure, the semiconductor device comprising a semiconductor substrate of a first conductivity type having a memory region; a first well of a second conductivity type located in the memory region; a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well; wherein the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer; wherein the first gate insulation layer and the second gate insulation layer are located above the second

well and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the second gate insulation layer and rests on the floating gate through the intermediate insulation layer; wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein the first transistor region includes a first voltage-type transistor that operates at a first voltage level of 1.8 - 3.3 V, the second transistor region includes a second voltage-type transistor that operates at a second voltage level of 2.5 - 5 V, and the third transistor region includes a third voltage-type transistor that operates at a third voltage level of 10 - 15 V; and wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

Response to Arguments

4. Applicant's arguments filed 08 July 2003 have been fully considered but they are not persuasive.

It is argued, at page 11 of the remarks, that "Claims 1-5,7-9,23, and 32 were rejected under 35 U.S.C. 103(a) as being unpatentable over HIRANO (5,652,450) in view of TAKEDA et al. (JP 09321156). Applicant notes that the Examiner cited specific

portions of the Takeda reference, which is in Japanese." However, Applicant mailed the Examiner a copy of the JP 09321156 reference in an IDS received 4/3/02. A copy of the relevant page of applicant's form 1449 is attached. Is applicant now taking the position that applicant had not read and understood this reference prior to applicant's listing it on the form 1449?

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In Re Fine* 837 F.2d 1071, 5 USPQ 2d 1596 (CAFC 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ 2d 1941 (CAFC 1992).

In this case, the teaching, suggestion, or motivation to utilize a split gate such as disclosed in JP-09321156 instead of the stacked gate used in Hirano comes from JP-09321156 which unequivocally states that the substitution is possible and that excess charge extraction from the floating gates during erase mode is less problematical when the split gate structure is substituted. It should be noted that the JP-09321156 reference directly compares the split gate to the stacked gate of Hirano and clearly indicates that the split gate solves the problem. A rough translation of JP-09321156 is available at the JPO website at:

http://www6.ipdl.jpo.go.jp/Tokujitu/PAJdetail.ipdl?N0000=80&N0120=01&N2001=2&N3001=H09-321156

The relevant portion reads:

> [0003] The memory cell (memory cell transistor) which constitutes a flash EEPROM is roughly classified into a stack TOGETO type and a split-gate type. The flash EEPROM using the stack TOGETO type memory cell does not have the function which chooses itself as each memory cell. Therefore, in case a charge is drawn out from a floating-gate electrode at the time of data elimination, even when the charge was extracted too much superfluously and the predetermined voltage (for example, 0V) for making a memory cell into non-switch-on is impressed to a control gate electrode, a channel field will be in switch-on. Consequently, the problem that the memory cell will always be in switch-on, and read-out of the memorized data becomes impossible, and the problem of the so-called superfluous elimination arise. In order to prevent superfluous elimination, a device needs to be required for an elimination procedure and it is necessary to control an elimination procedure by the circumference circuit of a memory device, or to control an elimination procedure by the external circuit of a memory device.
>
> [0004] The split-gate type memory cell was developed in order to avoid the problem of superfluous elimination in such a stack TOGETO type memory cell.

It is argued, at page 12 of the remarks, that "one of ordinary skill, in reading Hirano and Taketa, would realize that Hirano solves any problem relating to 'excess erasure' by the use of a 'peripheral circuit of the memory device or [emphasis added] by an external circuit connected to the memory device" However, Hirano offers two equally acceptable methods for solving the 'excess erasure' problem. JP-09321156 also offers these two methods: "[T]o [1] control an elimination procedure by the circumference circuit of a memory device, or [2] to control an elimination procedure by the external circuit of a memory device" (note paragraph 3). JP-09321156 then adds a third acceptable alternative: to use the "split-gate type memory cell [which] was developed in order to avoid the problem of superfluous elimination" (note paragraph 4) It would be reasonable to conclude that one of ordinary skill, in reading Hirano and JP-09321156, would realize that Hirano and JP-09321156 taken together solve any problem relating to 'excess erasure' by the use of a "peripheral circuit of the memory device," or by "an external circuit connected to the memory device," or by using the split-gate type memory cell.

It is argued, at page 12 of the remarks, that "a similar rationale used to overcome the rejection of claim 1 could also be used for [independent] claim 32." Applicant's use of subjunctive ("could") indicates that applicant understands that this is pure conjecture. Claim 32 is independent of claim 1. "Independent" means claim 1 claims features not found in claim 32, and vice versa. Because claim 1 claims features not found in claim 32 (features upon which patentability of claim 1 could be based) patentability of claim 1, in and of itself, is not reason to conclude claim 32 is patentable. Since applicant argues only patentability of claim 1 and makes no arguments concerning patentability of claim 32, there is simply no basis for reversing the rejection of claim 32.

It is argued, at page 13 of the remarks, that "a similar rationale used to overcome the rejection of claim 1 could also be used for [independent] claim 31." Applicant's use of subjunctive ("could") indicates that applicant understands that this is pure conjecture. Claim 31 is independent of claim 1. "Independent" means claim 1 claims features not found in claim 31, and vice versa. Because claim 1 claims features not found in claim 31 patentability of claim 1, in and of itself, is not reason to conclude claim 31 is patentable. Applicant's only argument for patentability of claim 31 is that Thomas 6,242,773 does not motivate combining certain features found in claim 31 as well as in Hirano 5,652,450 and JP-09321156. The examiner's position vis-à-vis patentability of claim 31 is laid out on page 7 and the first 14 lines of page 8 of the rejection mailed 6/17/02. The examiner stands on this rejection in the paper mailed 4/4/03 and in the present paper. Applicant

has not yet seen fit to respond to this rejection except to argue that "a similar rationale used to overcome the rejection of claim 1 could also be used for claim 31."

It is argued on page 13 with respect to claims 10-11,16-20,25, and 28, "The Examiner's addition of Nakamura and Ito do not overcome the examiner's rationale for the combination of Hirano and Takeda as discussed above," and again on page 14 with respect to claims 12-14 and 21, that "The Examiner's addition of Nakamura, Ito, and Thomas do not overcome the examiner's rationale for the combination of Hirano and Takeda as discussed above," and again on page 14 with respect to claim 8 that "The Examiner's addition of Lu does not overcome the examiner's rationale for the combination of Hirano and Takeda as discussed above." However, applicant does not argue separate patentability for claims 8,10-14,16-21,25, and 28. In the absence of argument, it is concluded that applicant believes that these claims are only patentable if claim 1 is patentable.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
08/2003

Minhloan Tran
Primary Examiner
Art Unit 2826